

## L-Edit Edit Modules Modules

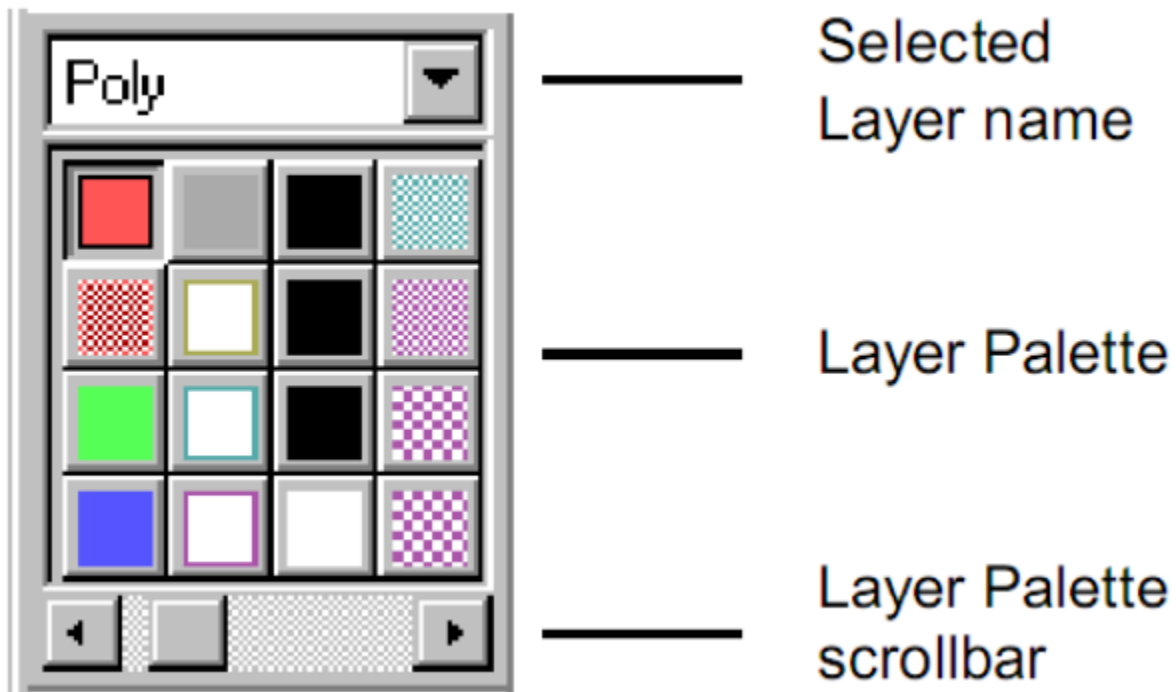
L-edit : Layout Editor

L-edit/DRC : Design Rule checker

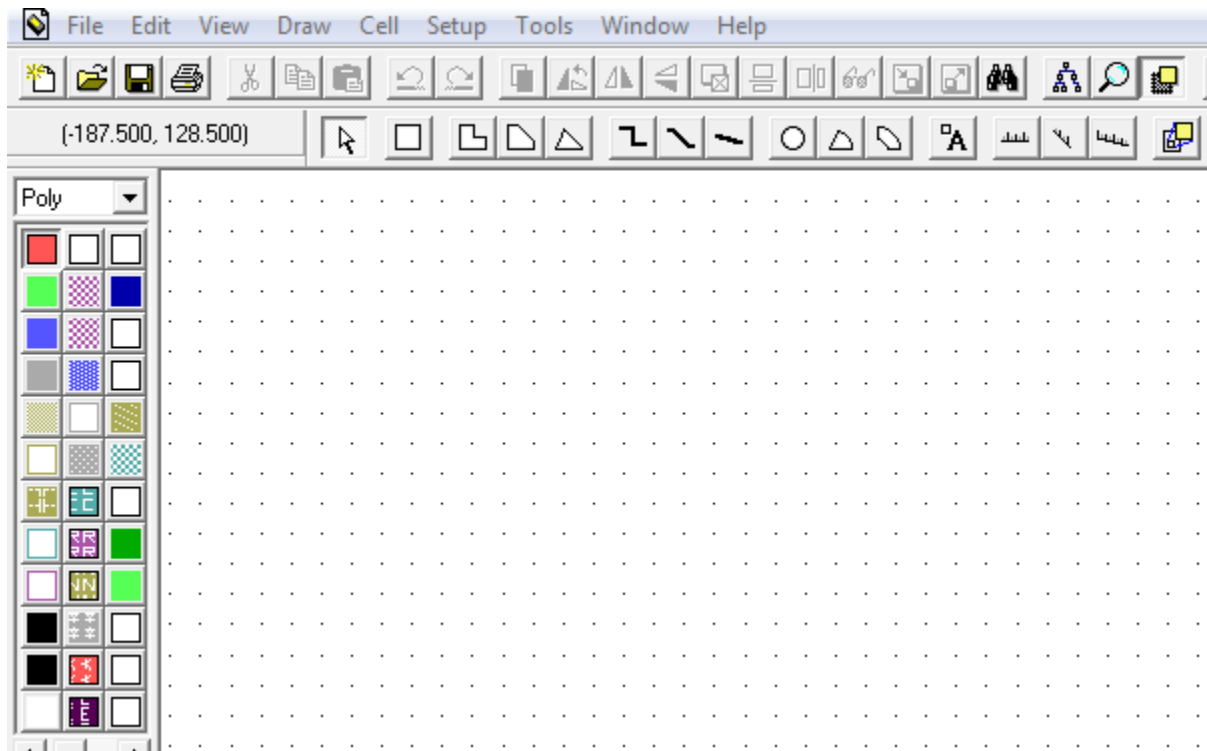
L-edit/extract : Spice File

### ***L-edit layout Editor :***

Thành phần chính trong Layout editor là các layer palette



Khung làm việc của L-edit:



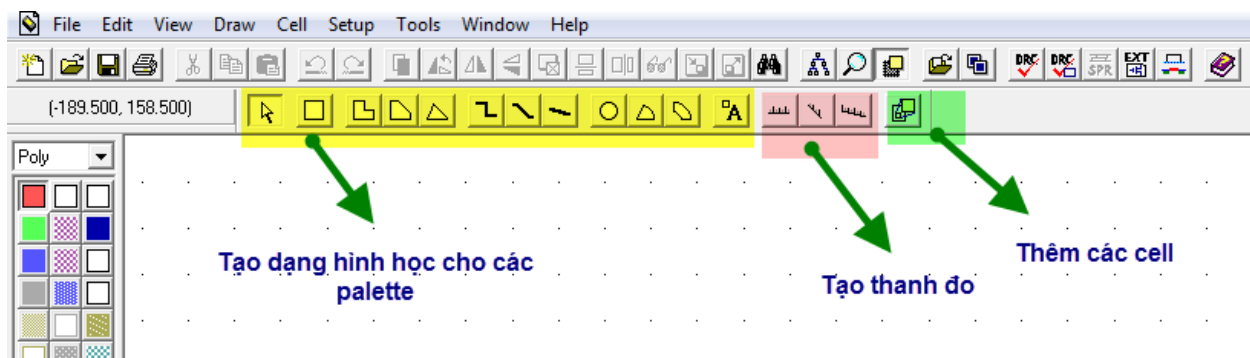
Things to Know:

Kích thước thường sử dụng trong layout là lamda ( $\lambda$ ). Mỗi hình vuông đơn vị trong cửa sổ làm việc của l-edit tương ứng với 1 lamda

Lambda ( $\lambda$ ) phải bằng 1 nửa chiều dài (L) (Chiều dài kênh dẫn Mosfet)

$$L=2*\lambda$$

## Thanh menuBar :



## Cài Đặt Thông số thiết kế :

MenuBar >>Setup >> Design >>

*Technology:*

**Setup Design**

Technology | Grid | Selection | Drawing

Technology name  
SCN 0.5u

Technology units  
☐ Microns   ☐ Millimeters   ☐ Centimeters  
☐ Mils   ☐ Inches   ☒ Other: Lambda

Technology setup  
☐ Maintain physical size of objects   ☒ Rescale the design

Lambda per Internal Unit  
 1 Internal Unit =  $\frac{1}{1000}$  Lambda

Lambda  
 1 Lambda =  $\frac{1}{4}$  Microns

OK Cancel

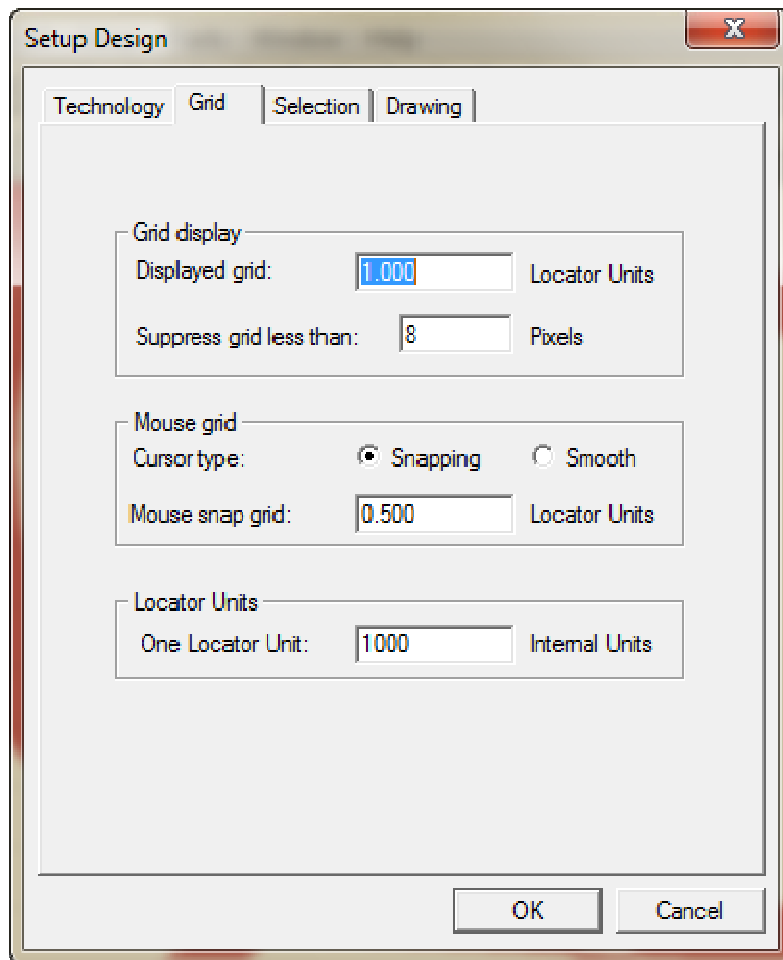
*Technology Name* : Tên của công nghệ được sử dụng. Giả sử ở đây dùng công nghệ 0.5u

*Technology units* : Chọn other, Nhập lambda. Với lựa chọn như thế này thì mỗi Units trong màn hình làm việc sẽ có giá trị bằng 1nm với công nghệ 0.5u, tương ứng với 1/1000 lambda

Hay nói cách khác 1 lambda ứng với 1000 đơn vị

Technology file có  $L=2 \times \text{lambda}$ . Với công nghệ 0.5u thì :  $L= 0.5 \text{ Microns}$   
 $\Rightarrow 1 \text{ Lambda} = 0.25 \text{ Micron}$

*Grid:*



Chọn thông số Displayed Grid và one locator Unit như hình

## CMOS Design Rules

Có 3 quy tắc chính về layout trong L-edit :

Minimum Width : Độ rộng tối thiểu cho mỗi layer

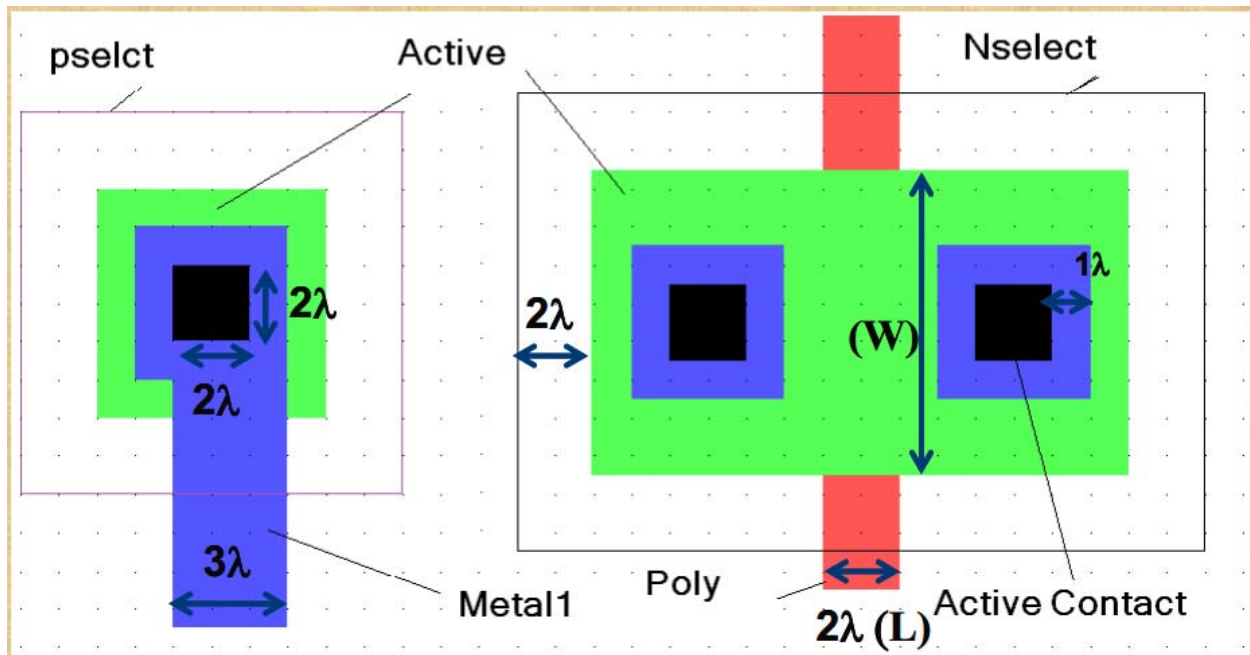
Spacing : Khoảng cách tối thiểu giữa các biên của 2 layer

Surround : sử dụng cho layer nằm bên trong 1 layer khác lớn hơn

Tất cả các lớp phải có Độ rộng và khoảng cách tuân theo quy luật nhất định. Trong slide này ta xác định luật khoảng cách theo lambda

## NMOS Layout:

Layers: Poly, Active, Metal Metal, Active Contact



L phải bằng  $2 \times \lambda$

Tất cả contacts phải có kích thước :  $2 \times \lambda \times 2 \times \lambda$

Minimum Metall width =  $3 \times \lambda$

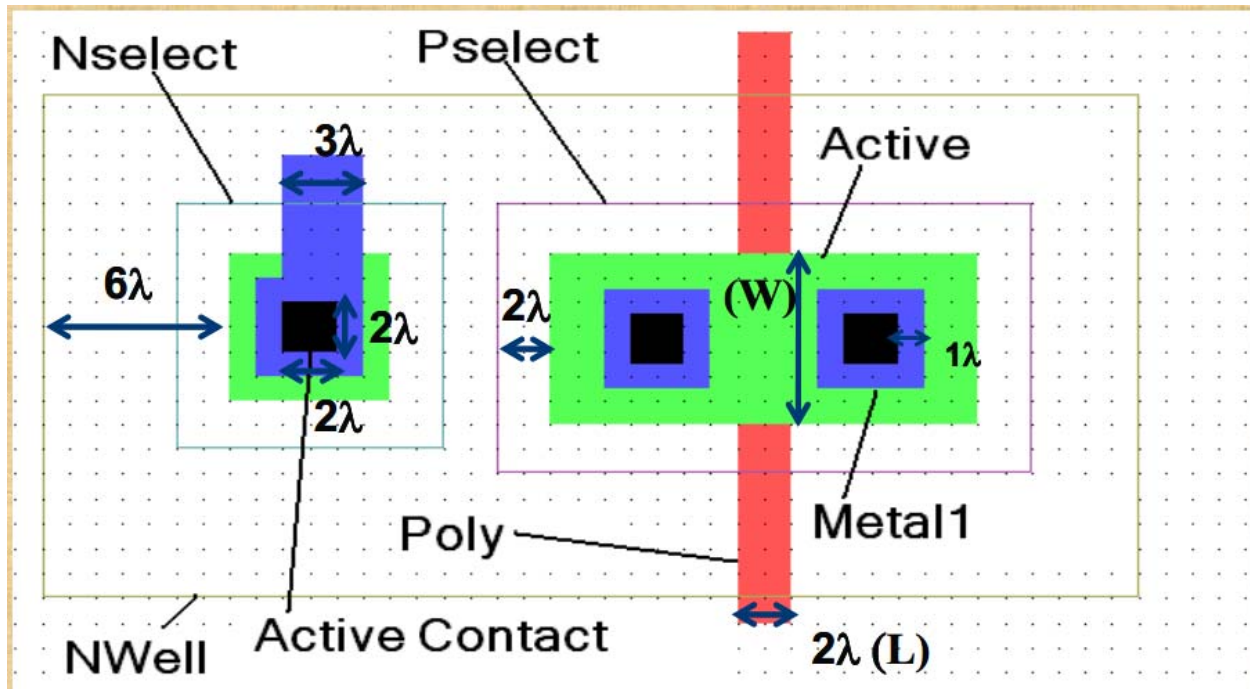
Khoảng cách tối thiểu từ active tới Nselect hoặc Pselect phải bằng  $2 \times \lambda$

Metal 1 Minimum surround Contact bằng  $\lambda$

W phải lớn hơn hoặc bằng  $3 \times \lambda$

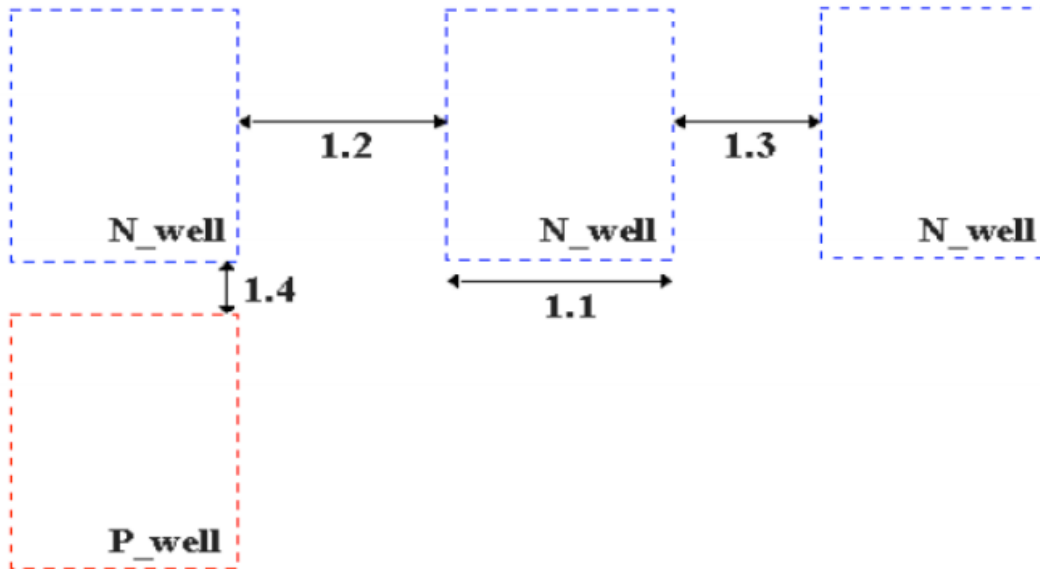
### PMOS layout:

Layers : Poly, Active, Nselect, Pselect, Metal, Active Contact, NWell



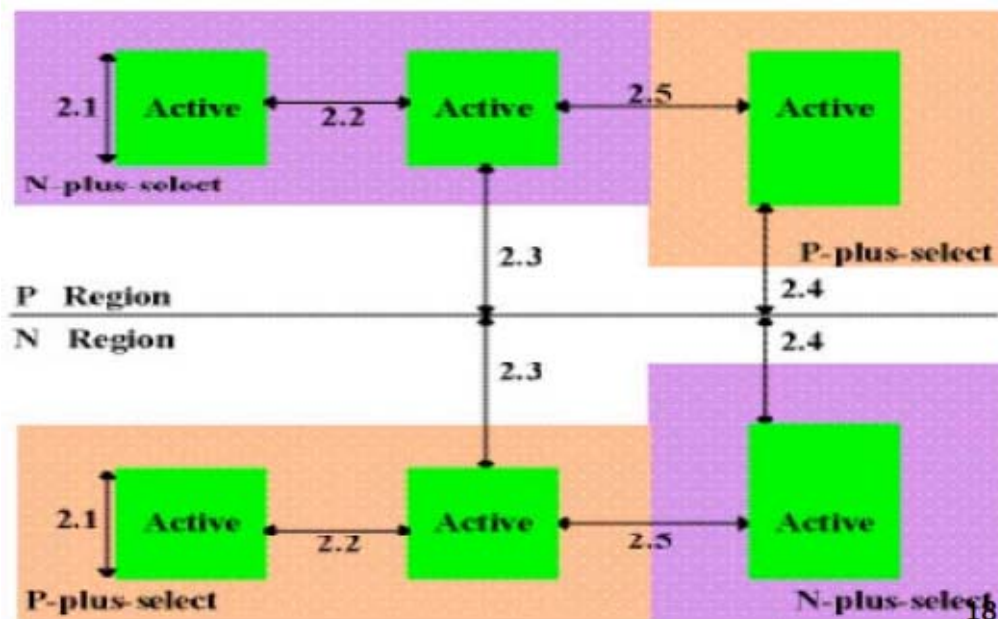
## CMOS Layout Rules - NWell

Rule	Description	Lambda		
		SCMOS	SUBM	DEEP
1.1	Minimum width	10	12	12
1.2	Minimum spacing between wells at different potential	9	18	18
1.3	Minimum spacing between wells at same potential	6	6	6
1.4	Minimum spacing between wells of different type (if both are drawn)	0	0	0



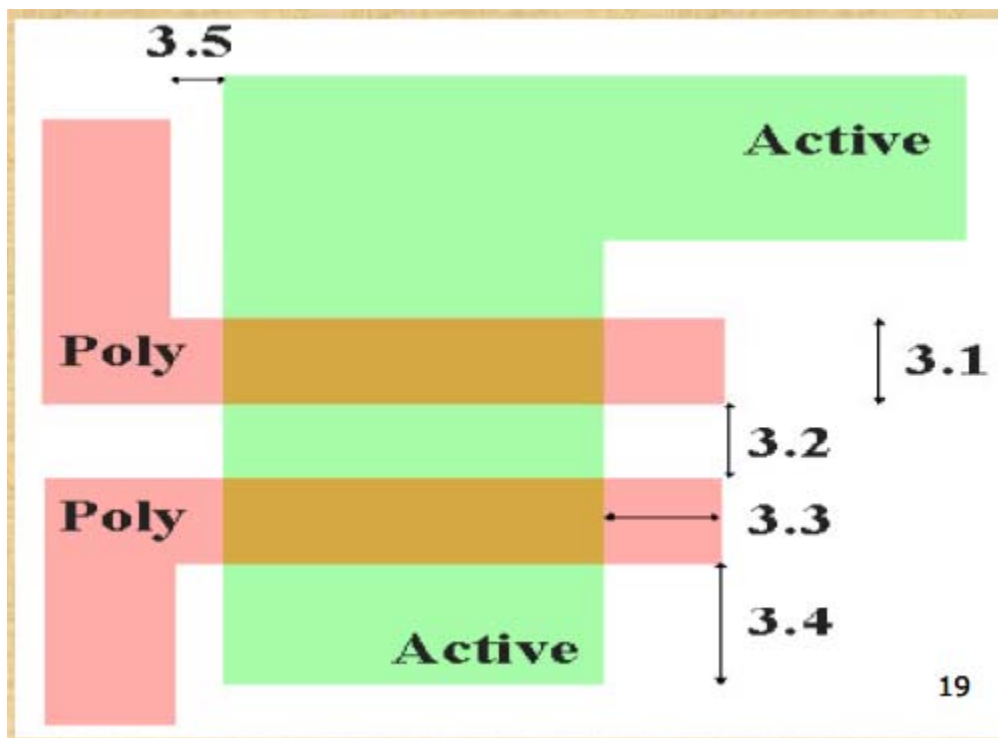
## CMOS Layout Rules - Active

Rule	Description	Lambda		
		SCMOS	SUBM	DEEP
2.1	Minimum width	3 *	3 *	3
2.2	Minimum spacing	3	3	3
2.3	Source/drain active to well edge	5	6	6
2.4	Substrate/well contact active to well edge	3	3	3
2.5	Minimum spacing between non-abutting active of different implant. Abutting active ("split-active") is illustrated under <a href="#">Select Layout Rules</a> .	4	4	4



## CMOS Layout Rules - Poly

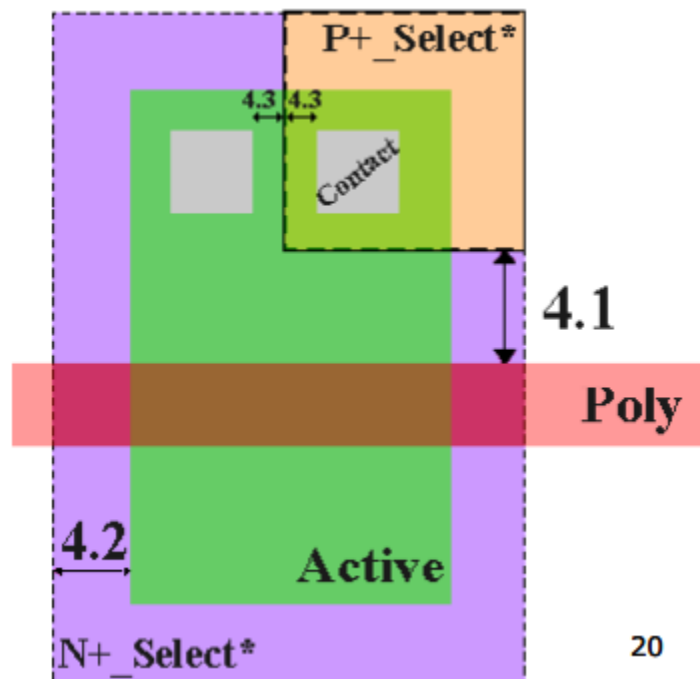
Rule	Description	Lambda		
		SCMOS	SUBM	DEEP
3.1	Minimum width	2	2	2
3.2	Minimum spacing over field	2	3	3
3.2.a	Minimum spacing over active	2	3	4
3.3	Minimum gate extension of active	2	2	2.5
3.4	Minimum active extension of poly	3	3	4
3.5	Minimum field poly to active	1	1	1



## CMOS Layout Rules - Select



Rule	Description	Lambda		
		SCMOS	SUBM	DEEP
4.1	Minimum select spacing to channel of transistor to ensure adequate source/drain width	3	3	3
4.2	Minimum select overlap of active	2	2	2
4.3	Minimum select overlap of contact	1	1	1.5
4.4	Minimum select width and spacing (Note: P-select and N-select may be coincident, but must <i>not</i> overlap) (not illustrated)	2	2 <sup>1</sup>	4



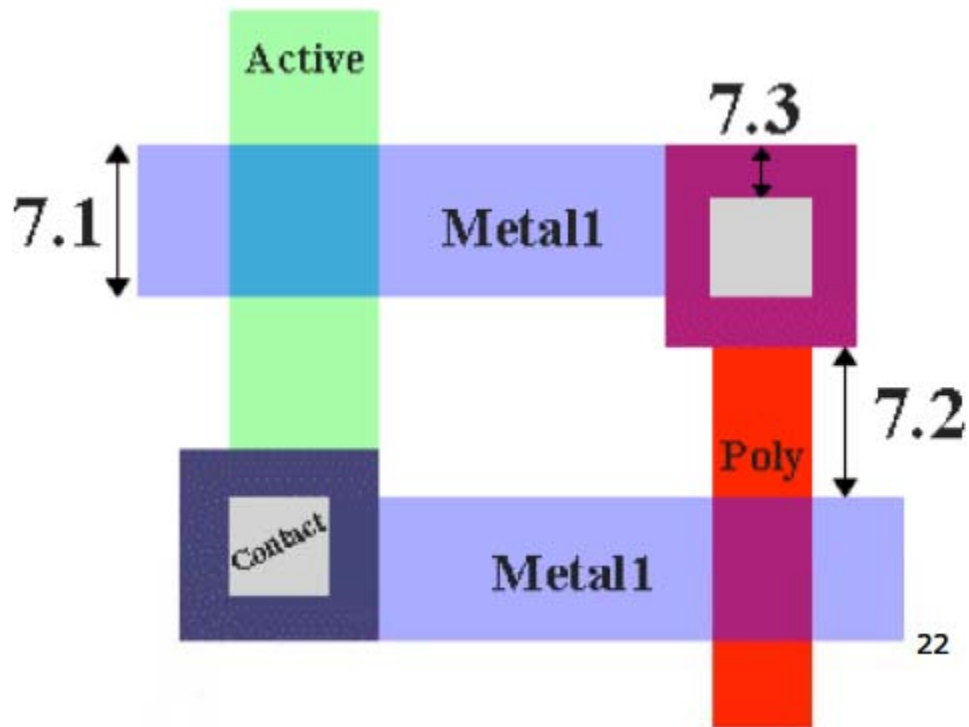
## CMOS Layout Rules - Contact to Poly & Contact to Active

Rule	Description	Lambda		
		SCMOS	SUBM	DEEP
5.1	Exact contact size	2x2	2x2	2x2
5.2	Minimum poly overlap	1.5	1.5	1.5
5.3	Minimum contact spacing	2	3	4
5.4	Minimum spacing to gate of transistor	2	2	2
6.1	contact size	2x2	2x2	2x2
6.2	Minimum active overlap	1.5	1.5	1.5
6.3	Minimum contact spacing	2	3	4
6.4	Minimum spacing to gate of transistor	2	2	2

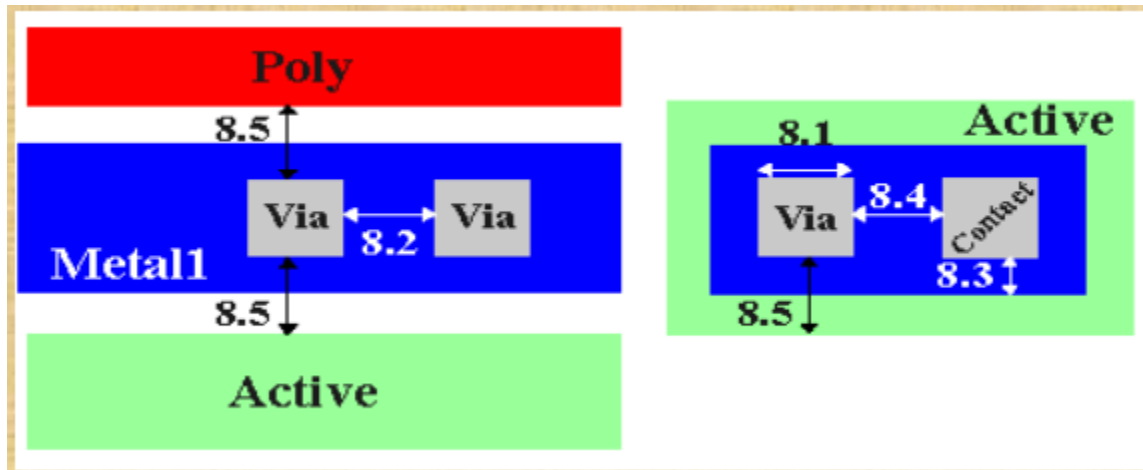
## CMOS Layout Rules - Metall

Rule	Description	Lambda		
		SCMOS	SUBM	DEEP
7.1	Minimum width	3	3	3
7.2	Minimum spacing	2	3	3
7.3	Minimum overlap of any contact	1	1	1
7.4	Minimum spacing when either metal line is wider than 10 lambda	4	6	6



## CMOS Layout Rules - Via

Rule	Description	Lambda					
		2 Metal Process			3+ Metal Process		
		SCMOS	SUBM	DEEP	SCMOS	SUBM	DEEP
8.1	Exact size	2 x 2	n/a	n/a	2 x 2	2 x 2	3 x 3
8.2	Minimum via1 spacing	3	n/a	n/a	3	3	3
8.3	Minimum overlap by metal1	1	n/a	n/a	1	1	1
8.4	Minimum spacing to contact for technology codes mapped to processes that do not allow <a href="#">stacked vias</a> (SCNA, SCNE, SCN3M, SCN3MLC)	2	n/a	n/a	2	2	n/a
8.5	Minimum spacing to poly or active edge for technology codes mapped to processes that do not allow <a href="#">stacked vias</a> (NOTE: list is not same as for 8.4)	2	n/a	n/a	2	2	n/a



## CMOS Layout Rules - Metal2

Rule	Description	Lambda					
		2 Metal Process			3+ Metal Process		
		SCMOS	SUBM	DEEP	SCMOS	SUBM	DEEP
9.1	Minimum width	3	n/a	n/a	3	3	3
9.2	Minimum spacing	3	n/a	n/a	3	3	4
9.3	Minimum overlap of via1	1	n/a	n/a	1	1	1
9.4	Minimum spacing when either metal line is wider than 10 lambda	6	n/a	n/a	6	6	8

